Landon Wardle

linkedin.com/in/landon-wardle | landonwardle.com | github.com/landonroxypal-repo
lwardle526306@gmail.com | 253-844-0966

Education

University of Washington Expected June, 2027
Double Major: Bachelor in Computer Engineering & Computer Science *GPA: 3.98*

Technical Skills

Languages: C/C++, SystemVerilog, MATLAB, C#, JavaScript, HTML/CSS, Java, Python
Frameworks & Libraries: React, Node.js, Express, Tailwind CSS, EJS
Tools & Platforms: ESP32, FPGA, KiCad, Quartus Prime, Oscilloscopes, VSCode, IntelliJ, Eclipse, Arduino IDE, MongoDB, Docker, YouTrack, ModelSim
Software Development: UML Diagrams, Test-Driven Development, Agile, Extreme Programming (XP), MVC

Projects

FPGA-based Smart Campus Parking Lot

C++, Node-RED, YOLO & OCR, Raspberry Pi, ESP32, DE10 FPGA *Mar 2025 – Present*

- Designing an embedded system containing 6 finite-state machines across a central **FPGA** and multiple **ESP32**s to manage gate control, capacity counting, lighting, and traffic congestion for a university parking garage.
- Building an **ALPR** pipeline on **Raspberry Pi 5** using **YOLOv8** and **OCR** to detect and validate license plates against a license plate database along with predicting garage capacity based off historical data.
- Deploying a **Node-RED** dashboard on a Raspberry pi 5 for system state visualization across all FSM modules.

Smart Plant Watering System (Herbinator)

C++, Distributed Hardware, PCB Design *Sep 2025 – July 2026*

- Engineered an FSM-based bare metal plant watering unit that communicated with a central **ESP32** microcontroller over a network via **HTTP**.
- Drove VPD-based automated watering decisions from capacitive soil moisture and DHT11 sensors through a DFR0523 pump; validated behavior after an 8-hour test run in **MATLAB** against .csv logs. Writes to SD card via **SPI**.
- Iterated the circuit design from pinout schematic to breadboard-**Arduino** prototype to a **KiCad** PCB, re-soldering components after fabrication to fix design errors.

16-bit Processor

DE2-115 FPGA, SystemVerilog, ModelSim, Quartus *May 2025 – Present*

- Designed a 16-bit processor with a six-instruction CISC ISA from scratch in **SystemVerilog** (NO-OP, Add, Subtract, Load, Store, Halt); extending it with jump, conditional jump, and subroutine handling.
- Validated the design with **test-driven SystemVerilog** testbenches in **ModelSim**, then synthesized in **Quartus Prime** and deployed to a DE-10 **FPGA**.

Suave Medical Wellness Website

Tailwind CSS, Node.js, React, Express, MongoDB *July 2026 – September 2026*

- Developed a company website that showcases company services and allows the owner to edit website content, containerized with **Docker** for deployment.
- Architected on the MERN stack with **MVC** Model 2 and styled in **Tailwind CSS**. Delivered across 1-week sprints, practiced **Agile** and **Extreme Programming** during sprints.

Extracurricular

IEEE UWT Branch

Projects and professional networking *Oct 2025 – Present*

- Vice Chair for 2026-2027, planning branch events for the summer and fall quarters.
- Represent the branch at IEEE Student Activities Committee and EXCOM meetings, discussing IEEE Seattle Section activities and connecting members with professionals.

ICPC/PSPC

Programming Competitions

- Solved algorithmic challenges in **Java** under strict time and memory limits at ICPC (Fall) and PSPC (Winter, Spring); placed second at PSPC Spring 2026.